

MS-7085

Version 0C

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CPU:

Intel LGA775 CPU

System Chipset:

Intel 915GV (North Bridge)

Intel ICH6 (South Bridge)

On Board Chipset:

BIOS -- FWH EEPROM

AC'97 Codec -- ADI1981B

LPC Super I/O -- SMSC LPC47M287

LAN -- Realtek 8101L

CLOCK -- ICS954119

Main Memory:

DDR 1 * 2 (Max 2GB)

Expansion Slots:

PCI SLOT * 1

Intersil PWM:

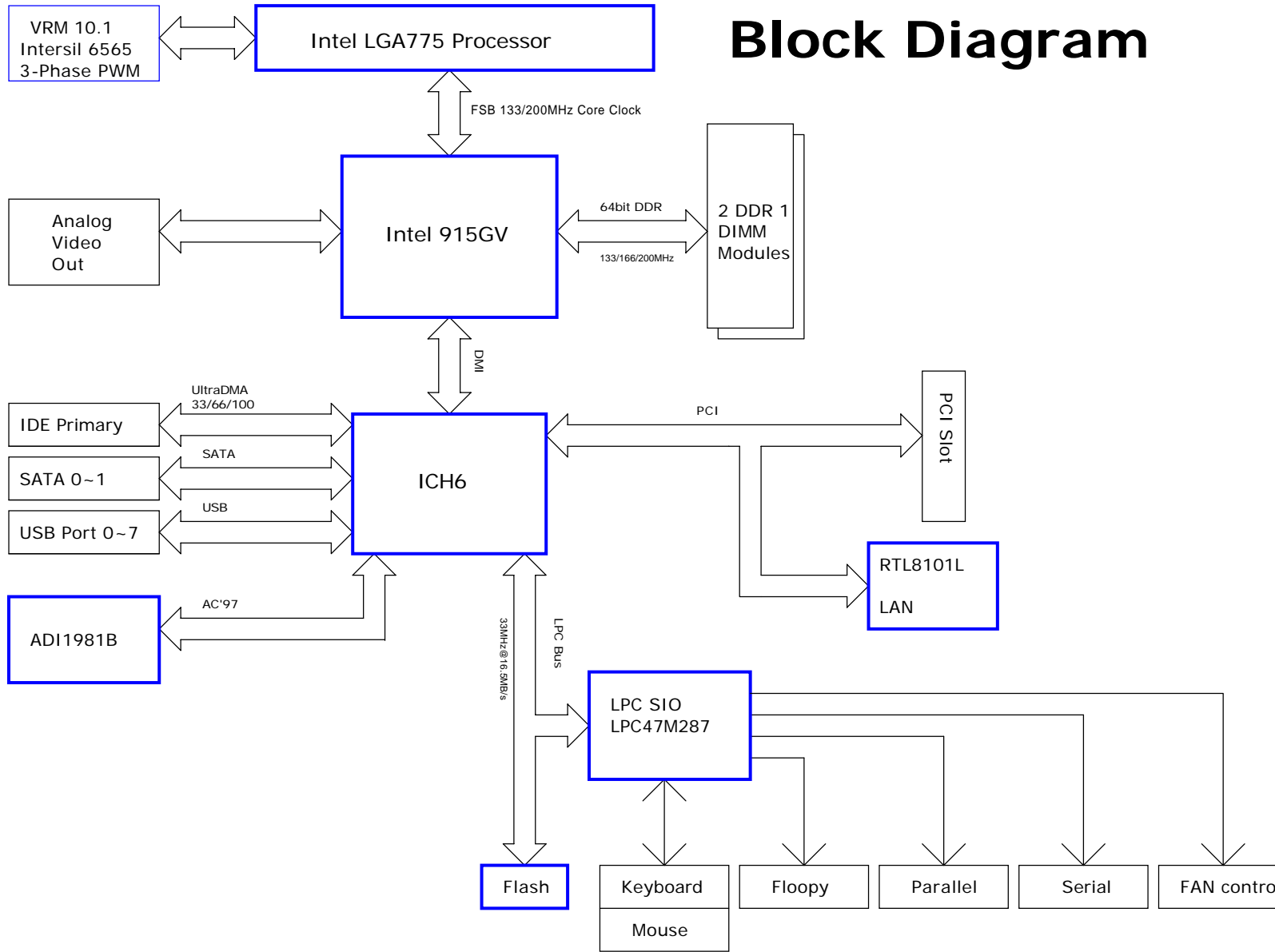
Controller: HIP6565 3 Phase

Driver: HIP6602B * 1 + HIP6601B * 1

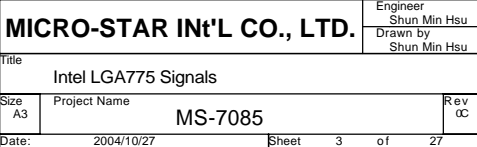
PCI Routing Table

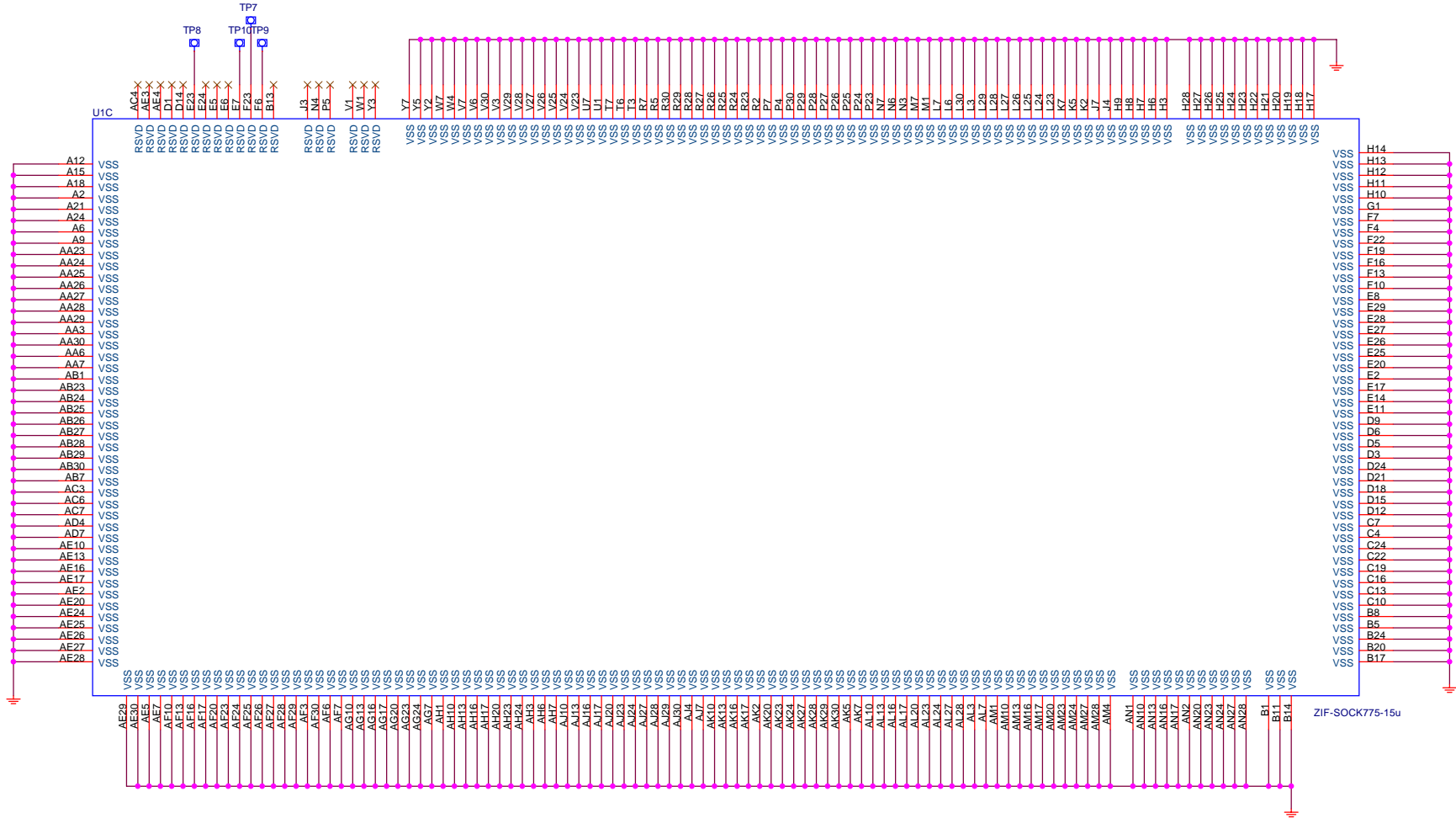
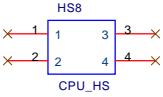
PCI Device	IDSEL	REQ/GNT	INTERRUPT
PCI Slot 1	AD16	1	A
RTL8101L LAN	AD29	3	F

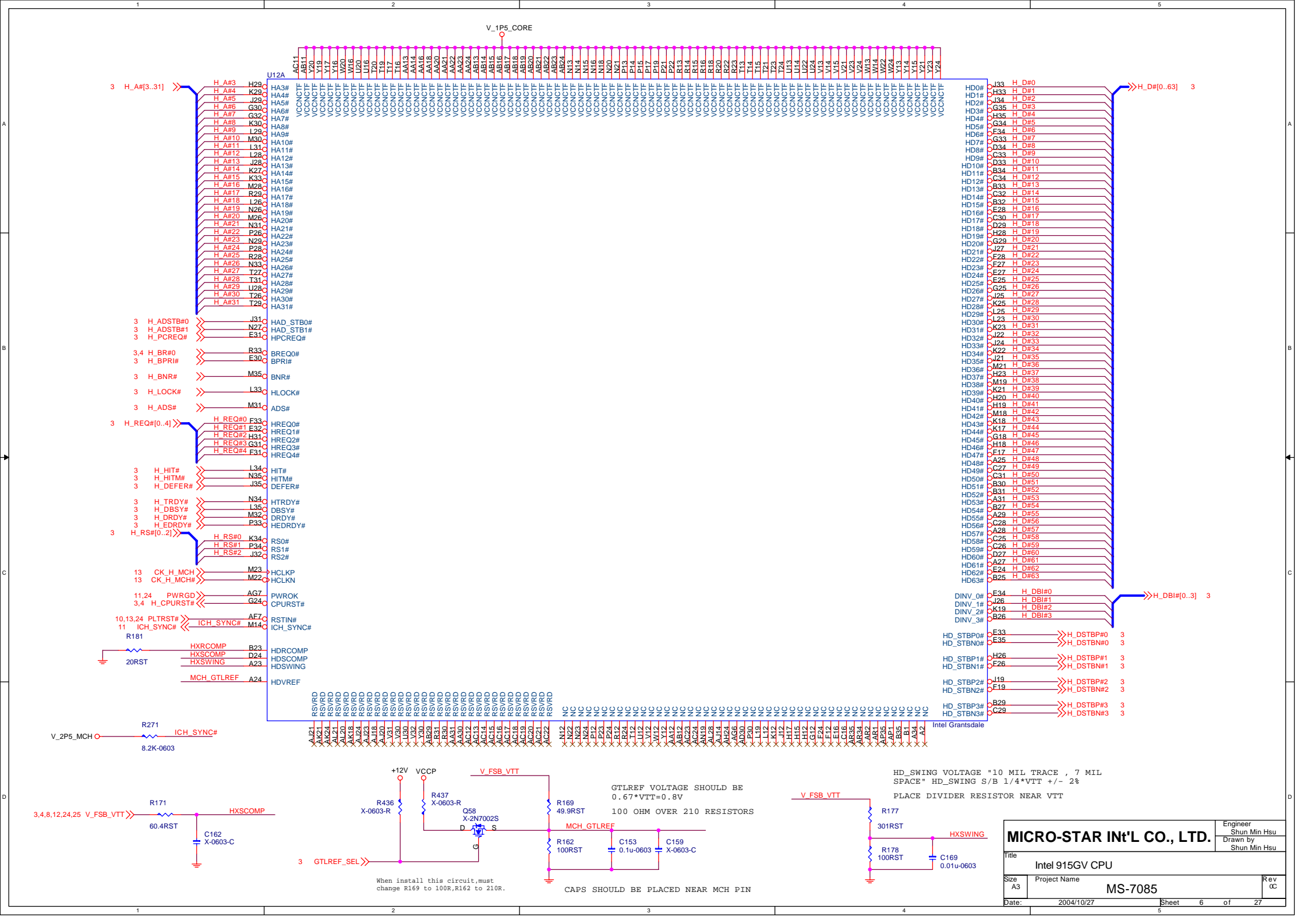
MICRO-STAR INT'L CO., LTD.		Engineer Shun Min Hsu
Title COVER SHEET		Drawn by Shun Min Hsu
Size A3	Project Name MS-7085	Rev 0C
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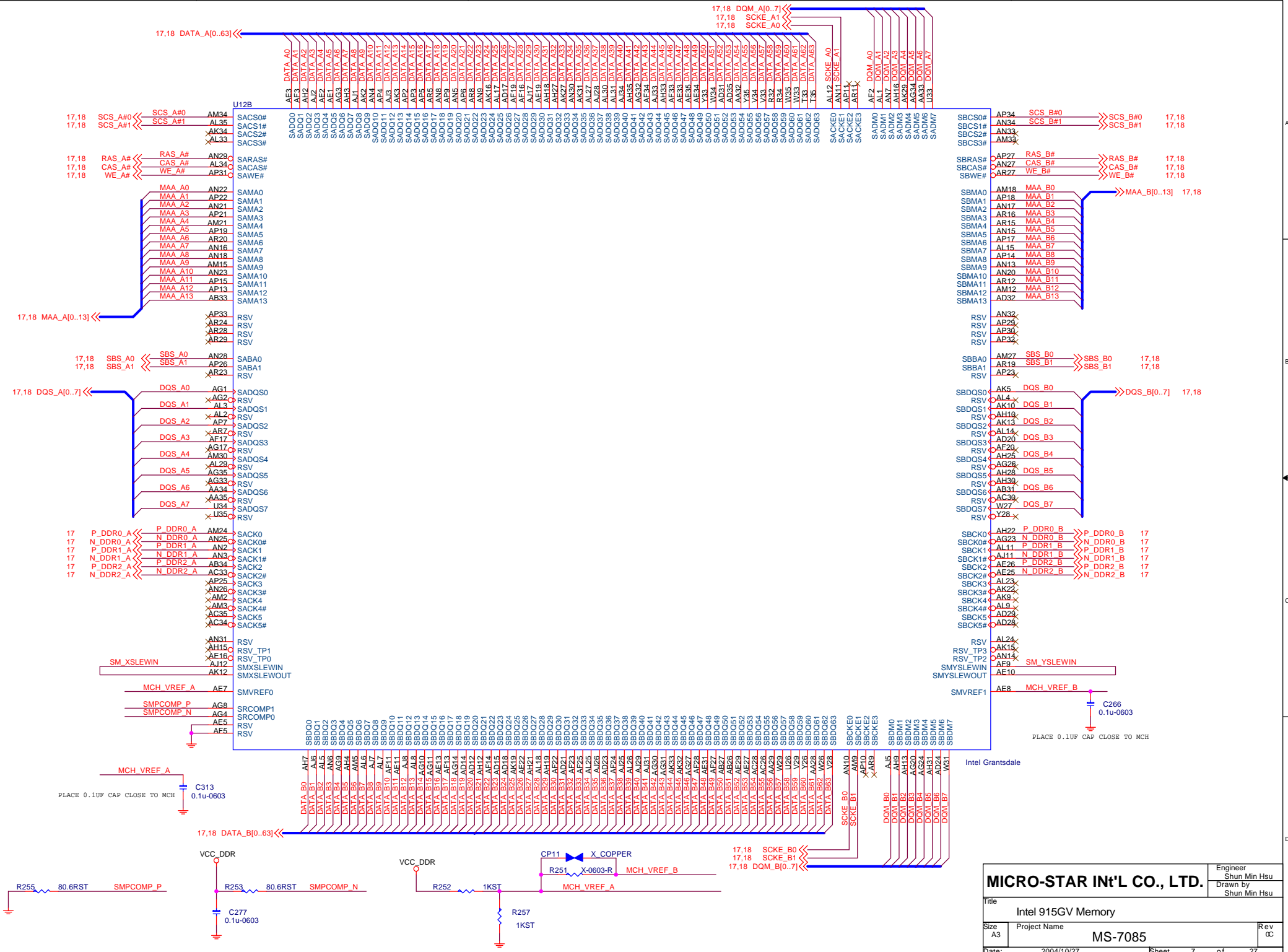


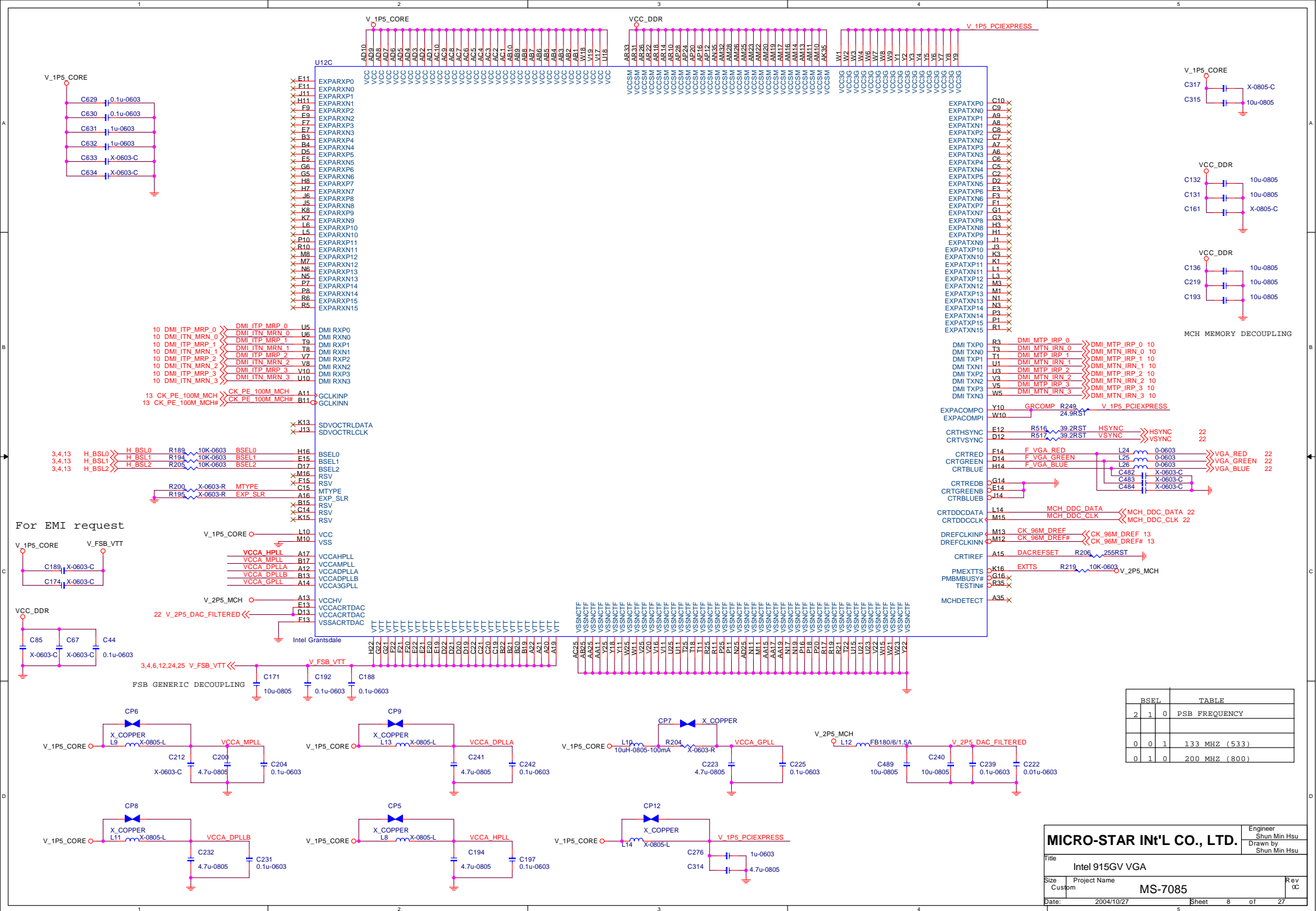
Block Diagram

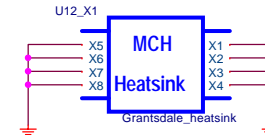












MICRO-STAR INT'L CO., LTD.			Engineer Shun Min Hsu	
Title Intel 915GV GND			Drawn by Shun Min Hsu	
Size A3	Project Name MS-7085			Rev 00
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U12_41
HS-HOOK-L



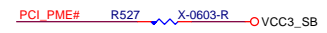
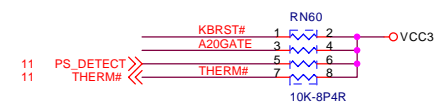
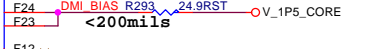
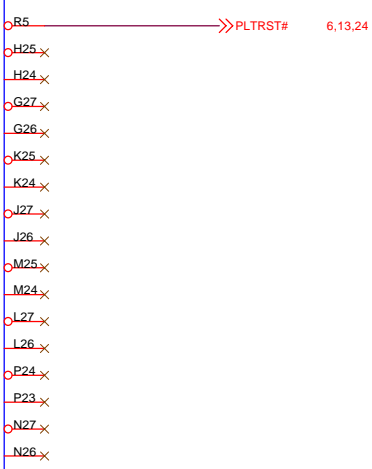
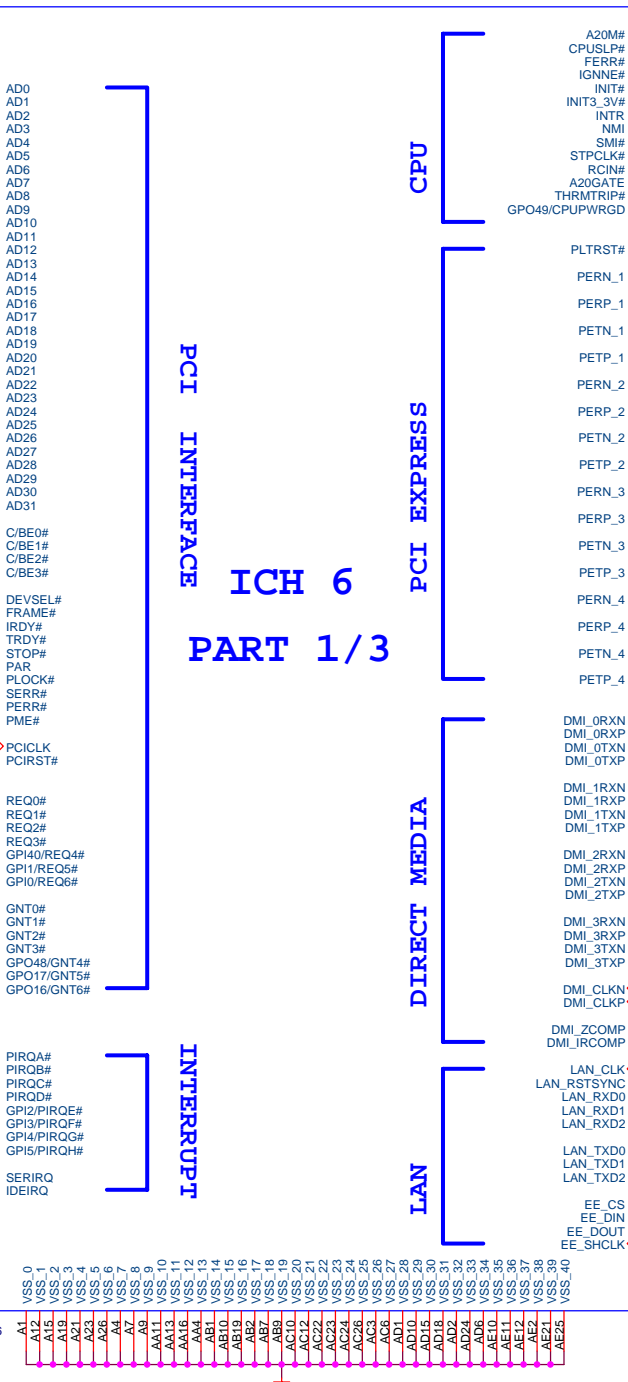
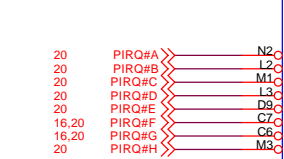
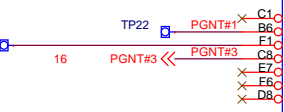
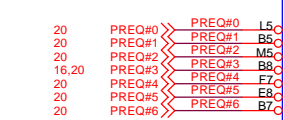
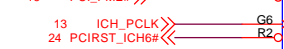
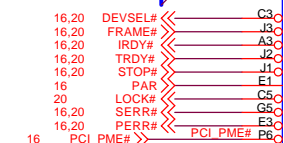
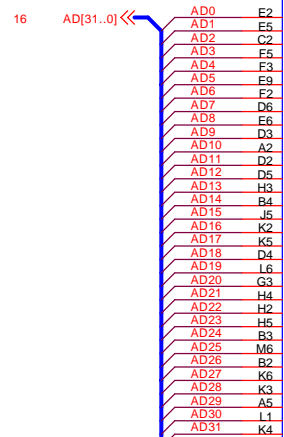
U12_42
HS-HOOK-L



U12_43
HS-HOOK-L

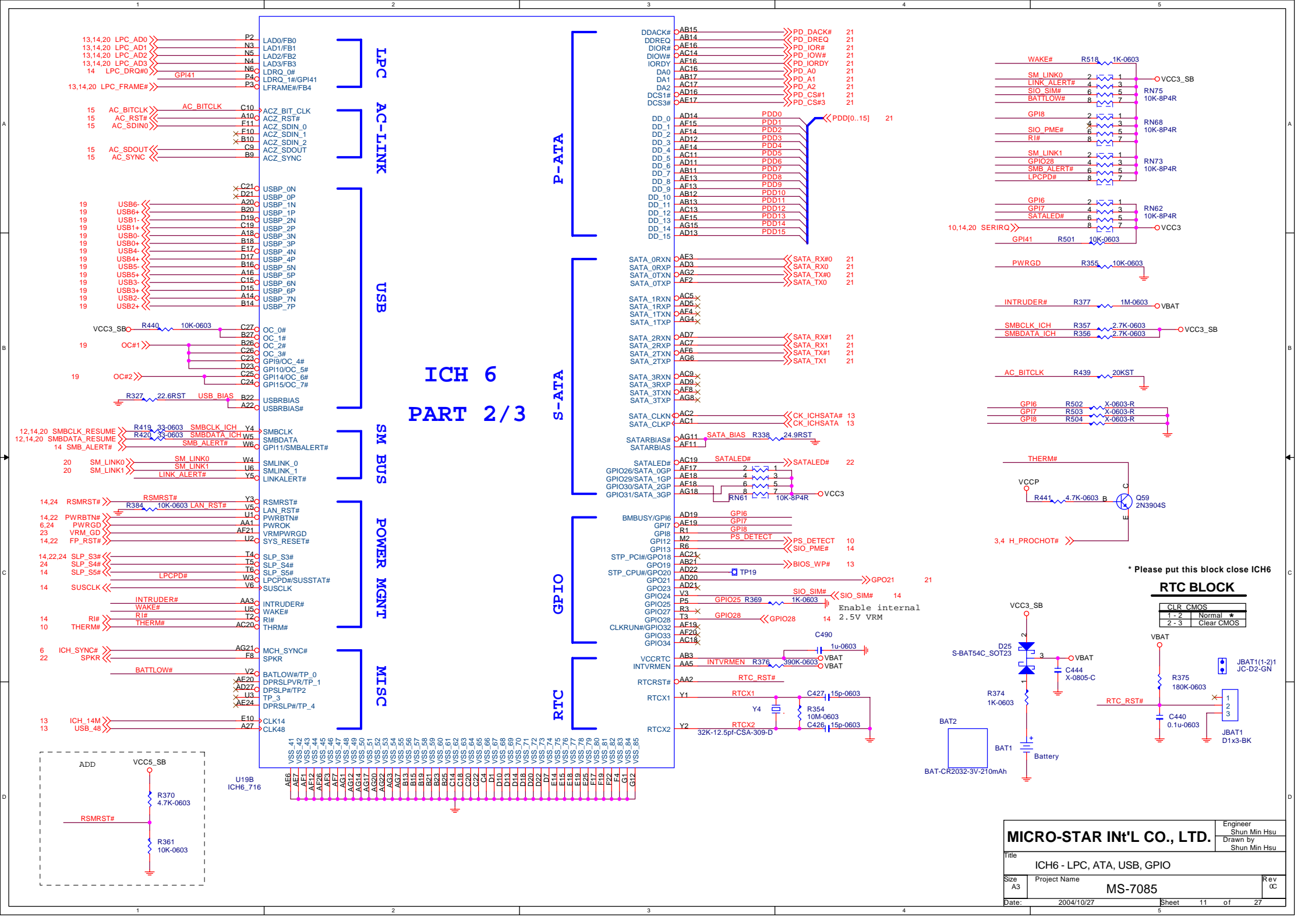


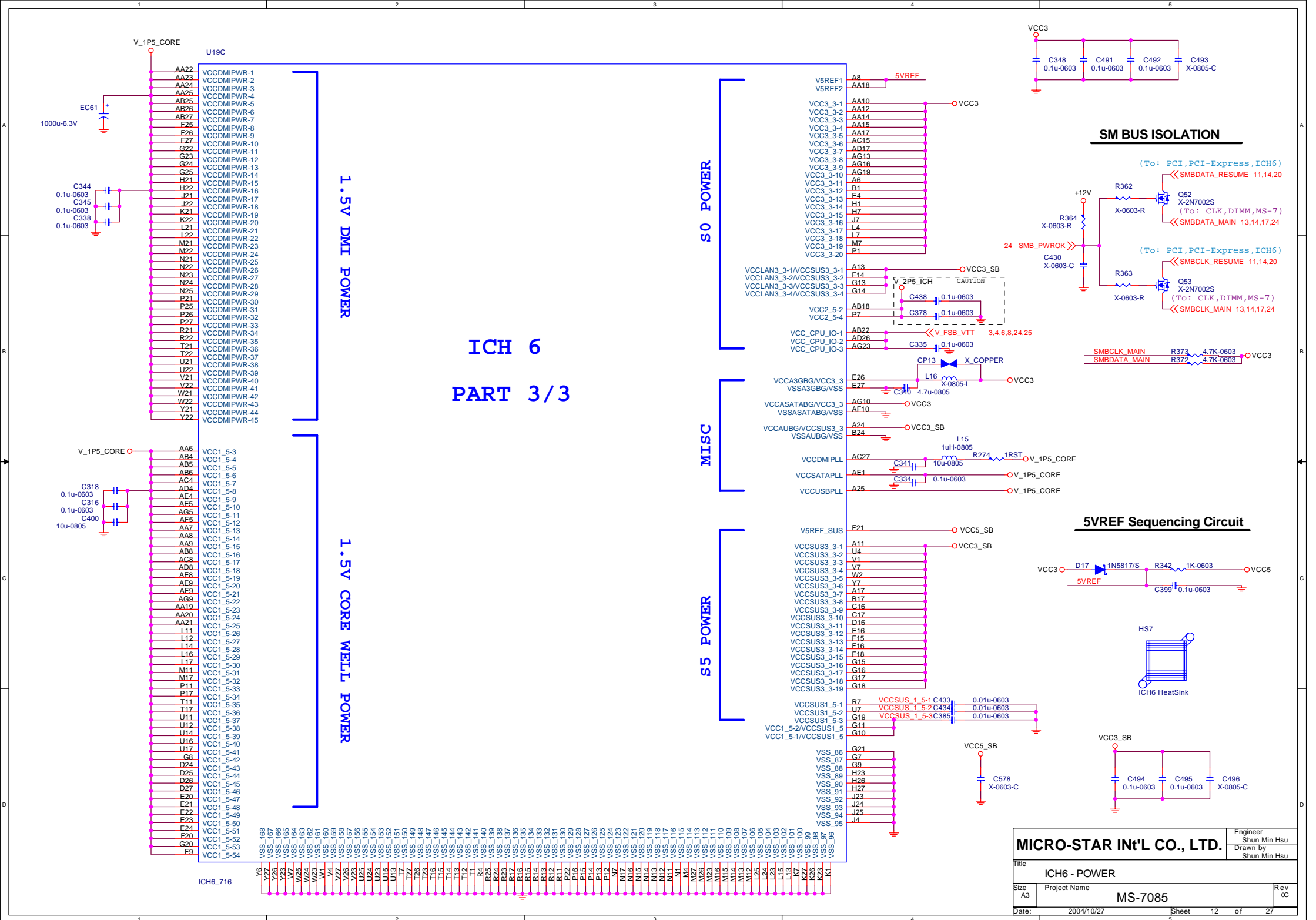
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HS-HOOK-L

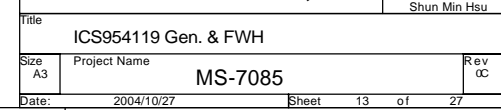


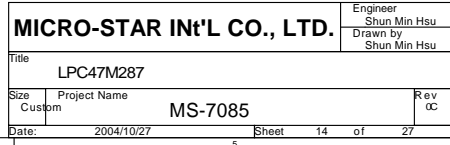
DMI Interface
Trace width 5 mils & 7 mils space.
GMCH breakout space 5 mils, length < 250 mils
Length matching < 5 mils
Trace Length 2" to 11"

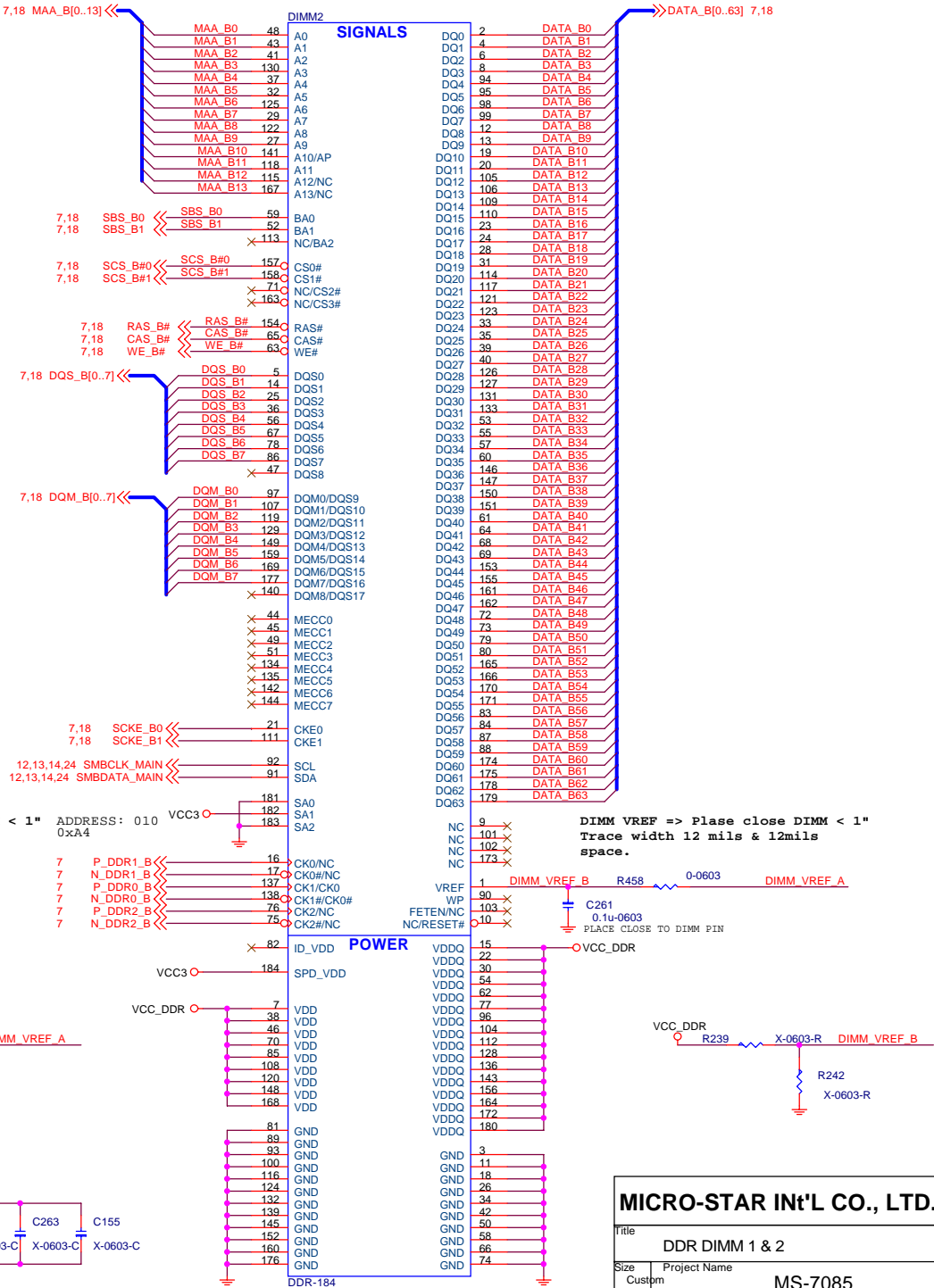
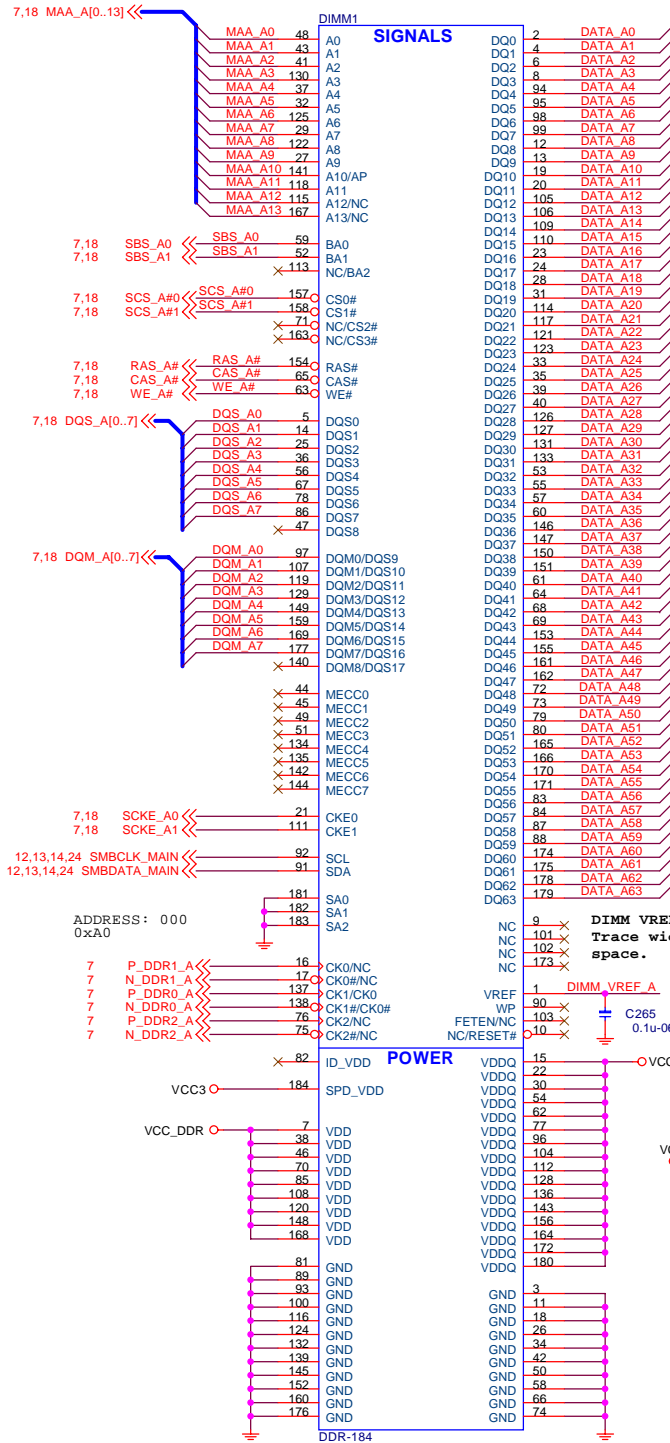
MICRO-STAR INT'L CO., LTD.		Engineer Shun Min Hsu	
Title ICH6 - PCI, DMI, CPU, IRQ		Drawn by Shun Min Hsu	
Size A3	Project Name MS-7085	Rev 00	
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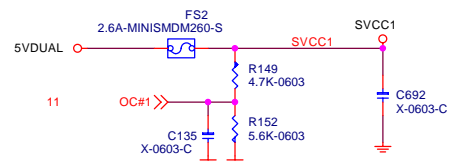


MICRO-STAR IN'L CO., LTD.

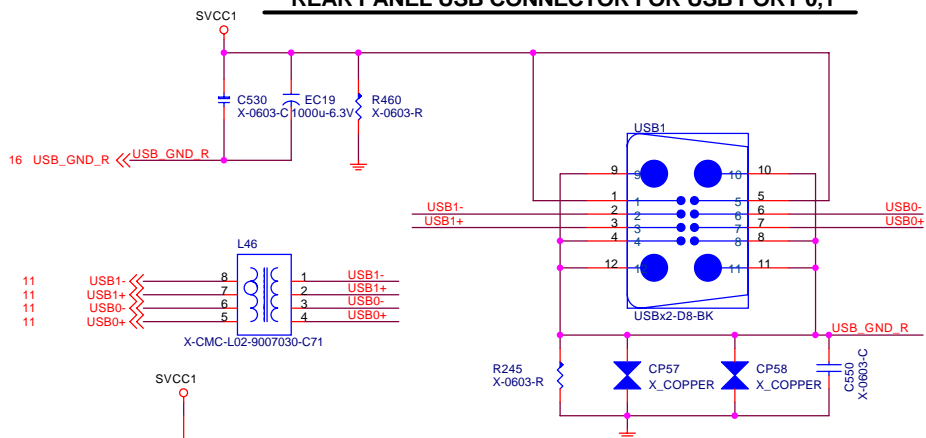
Engineer
Shun Min Hsu
Drawn by
Shun Min HsuTitle
DDR DIMM 1 & 2Size
Custom Project Name
MS-7085

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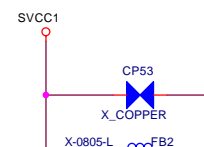
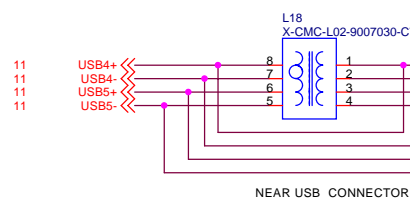
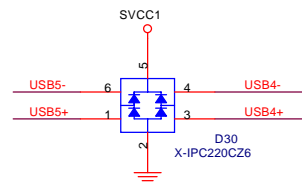
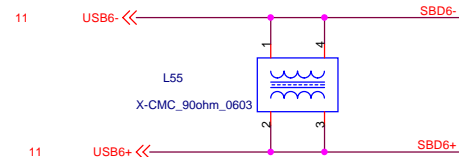
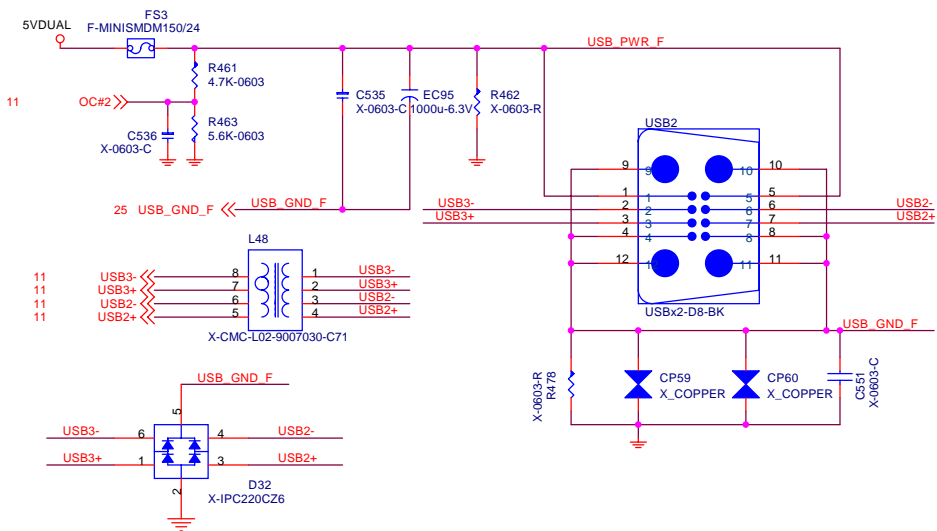
POWER CIRCUIT FOR USB PORT 0,1,2,3 (REAR)



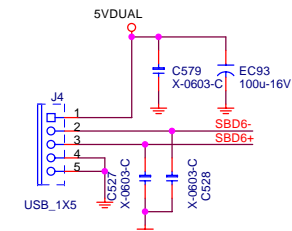
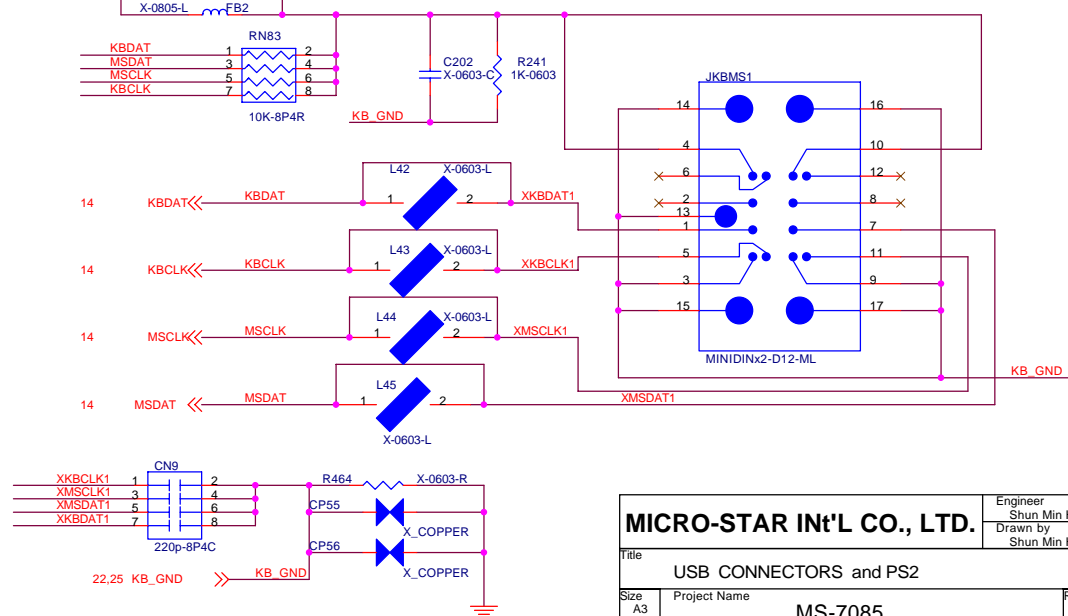
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



PS/2 KeyBoard / Mouse



J4 only for PCMCIA

MICRO-STAR INT'L CO., LTD.

USB CONNECTORS and PS2

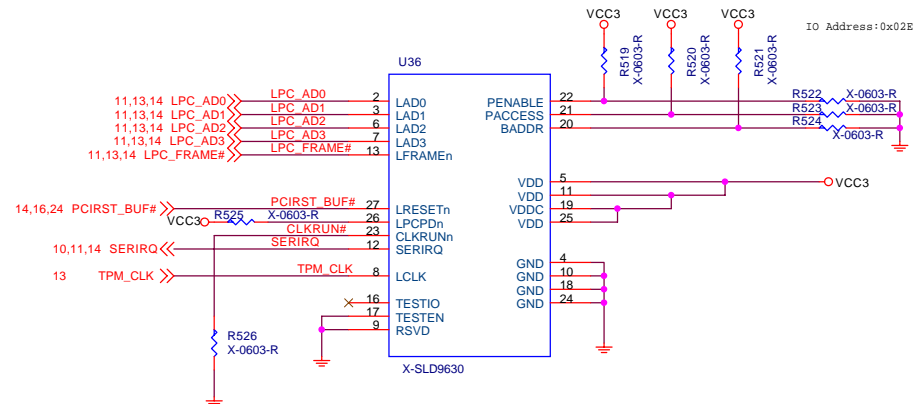
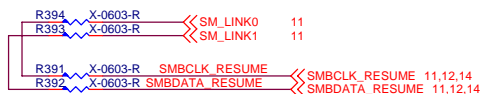
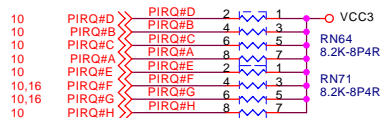
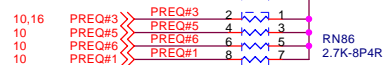
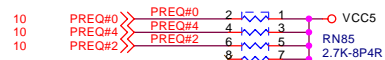
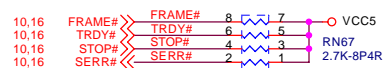
Size A3 Project Name MS-7085

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Engineer
Shun Min Hsu
Drawn by
Shun Min Hsu

Rev 00

PCI PULL-UP / DOWN RESISTORS



SERIAL ATA CONNECTOR LEGEND

Signal	Component	Value	Signal	Pin	Color
SATA_TX0	C416	0.01u-0603	SATA_CTX0	1	Blue
SATA_TX#0	C413	0.01u-0603	SATA_CTX#0	2	Red
SATA_RX#0	C415	0.01u-0603	SATA_CRX#0	4	Blue
SATA_RX0	C412	0.01u-0603	SATA_CRX0	5	Red

SATA1

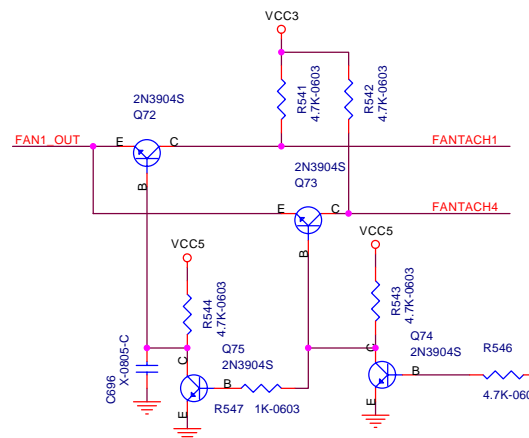
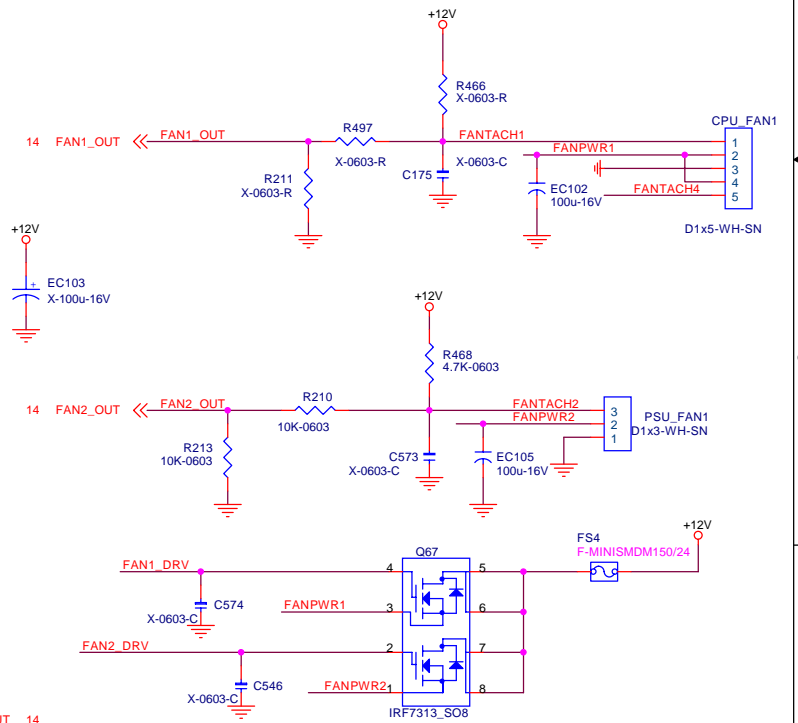
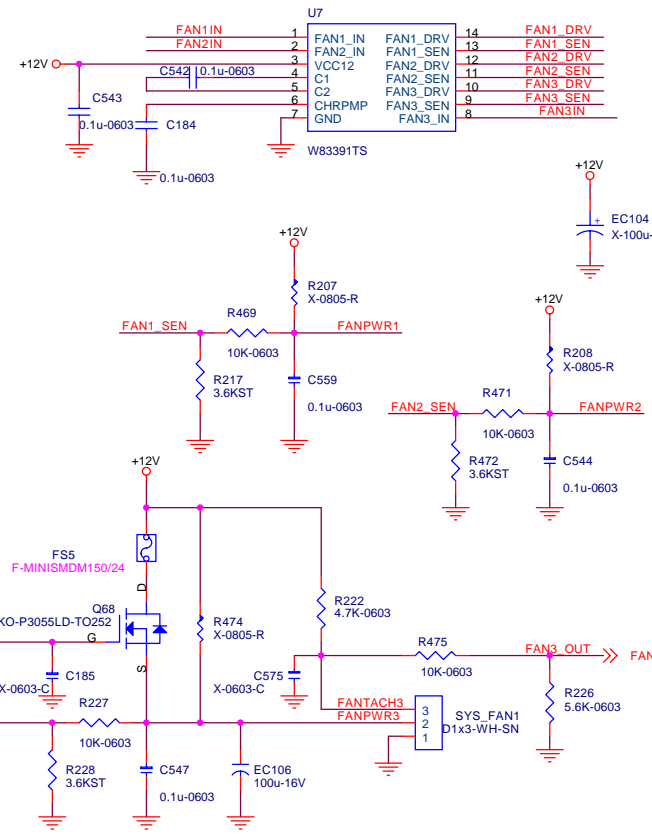
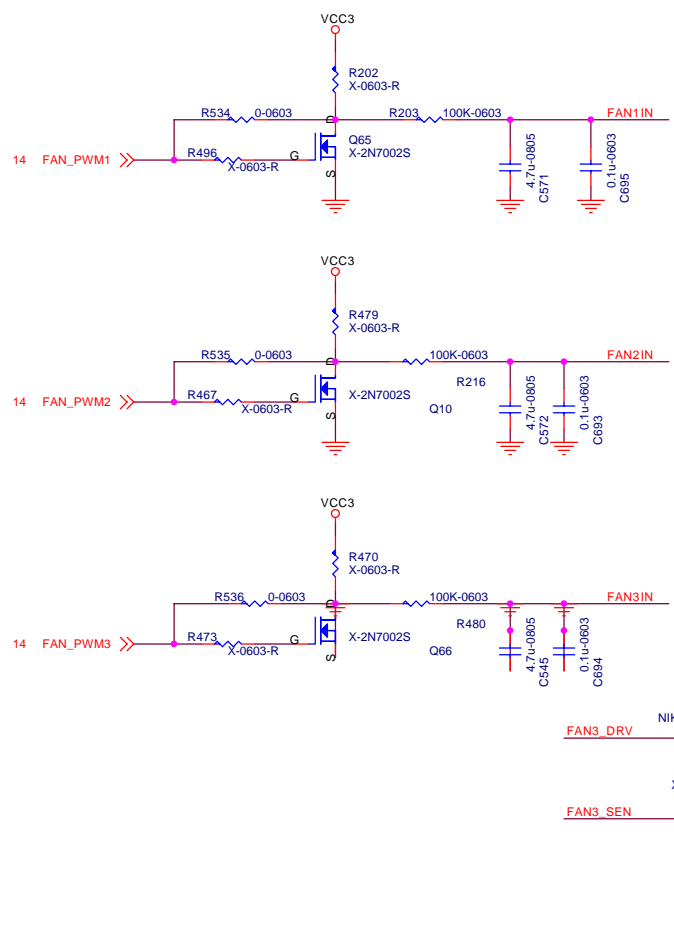
1 GND
2 HT+
3 HT-
4 GND
5 HR-
6 HR+
7 GND

SATA_BLACK

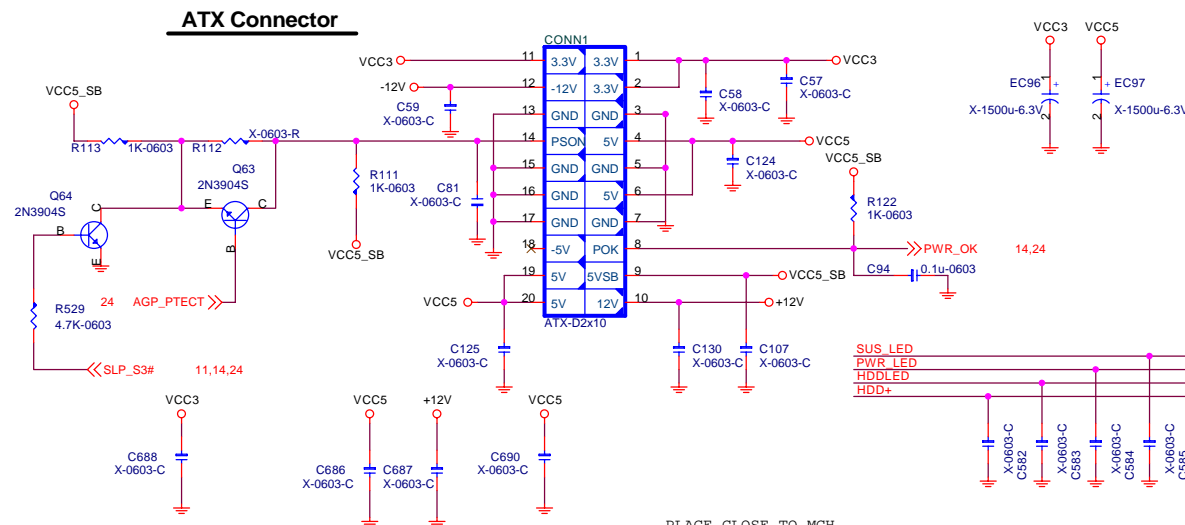
SATA2

1 GND
2 HT+
3 HT-
4 GND
5 HR-
6 HR+
7 GND

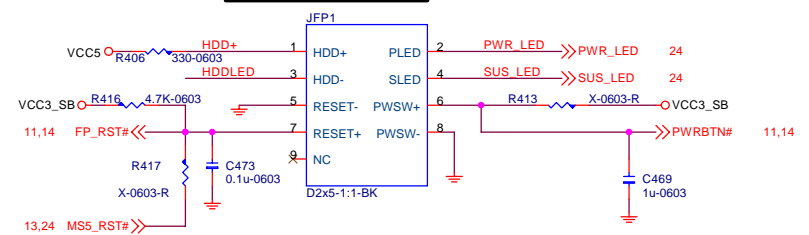
SATA_BLACK

[illegible]

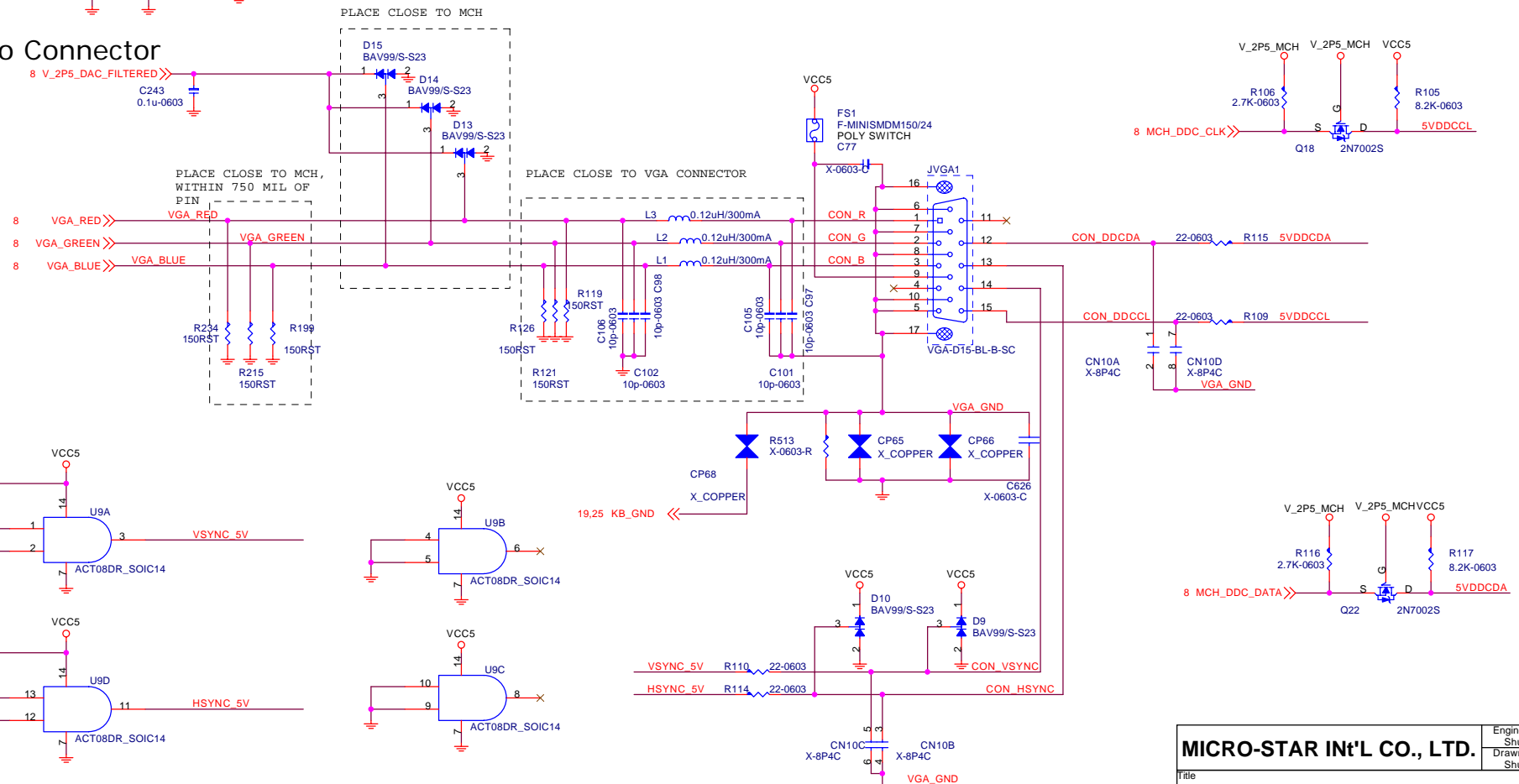
ATX Connector



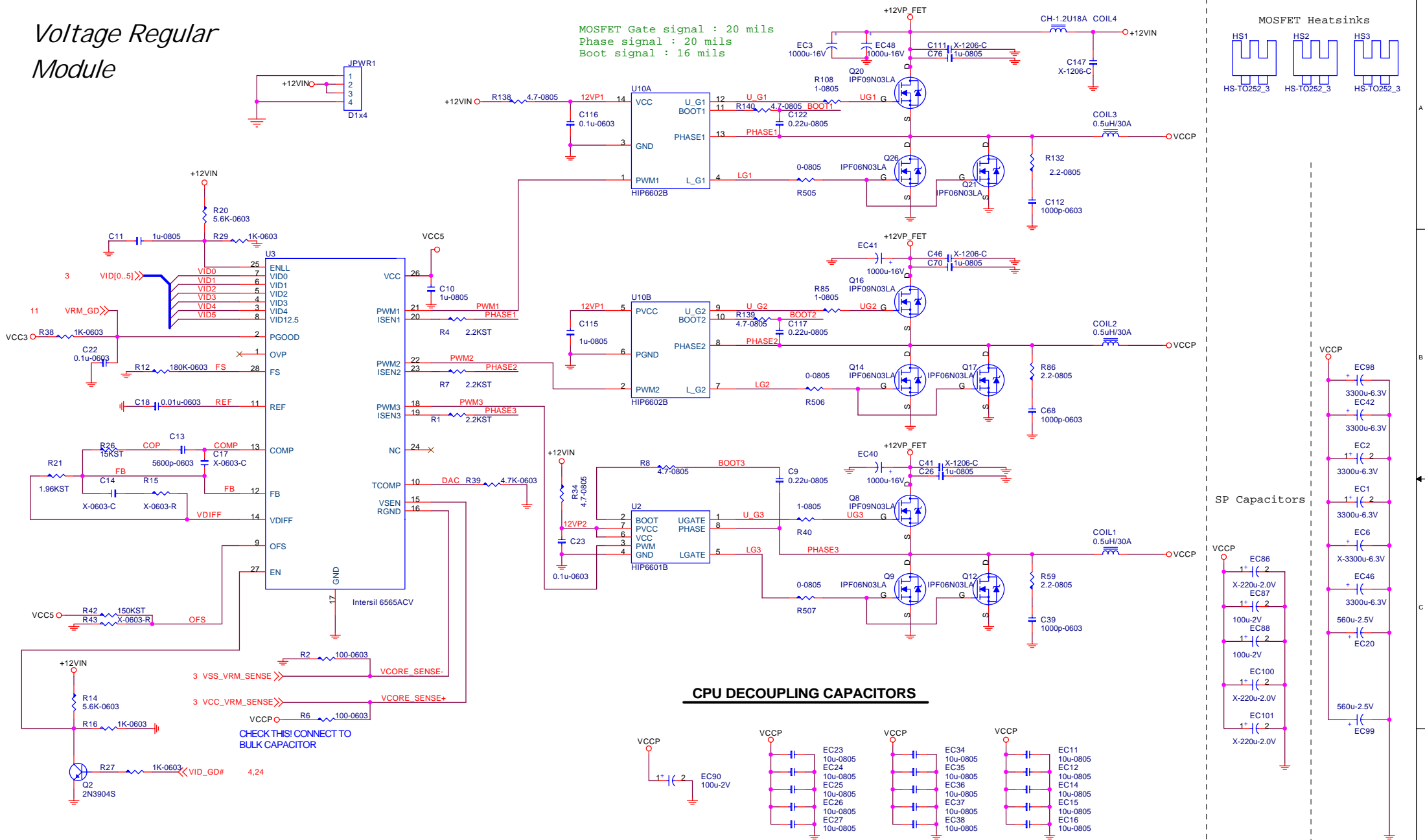
Intel Front Panel



Video Connector



Voltage Regular Module



MICRO-STAR INT'L CO., LTD.			Engineer Shun Min Hsu
Title VRM10.1 Intersil 6565 3Phase			Drawn by Shun Min Hsu
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ACPI Controller

3VSB MODE SELECT

3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

VDIMM LINEAR OR PWM SELECT

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

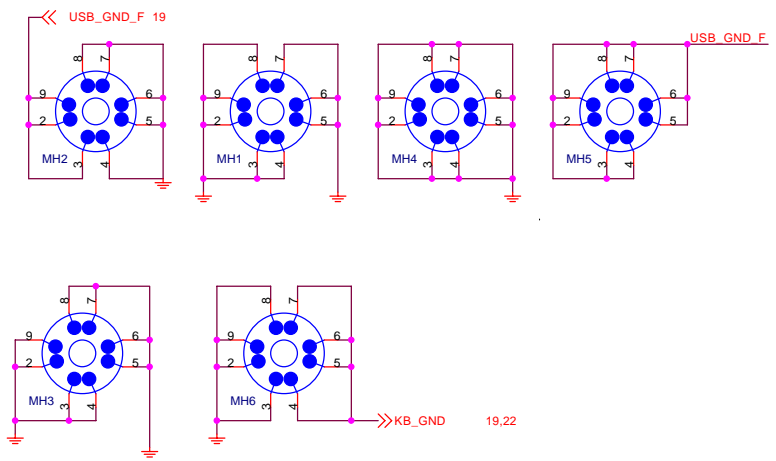
AGP POWER

5V DUAL Power

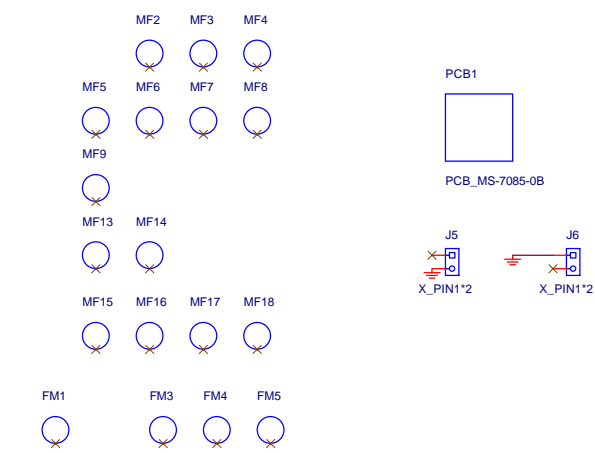
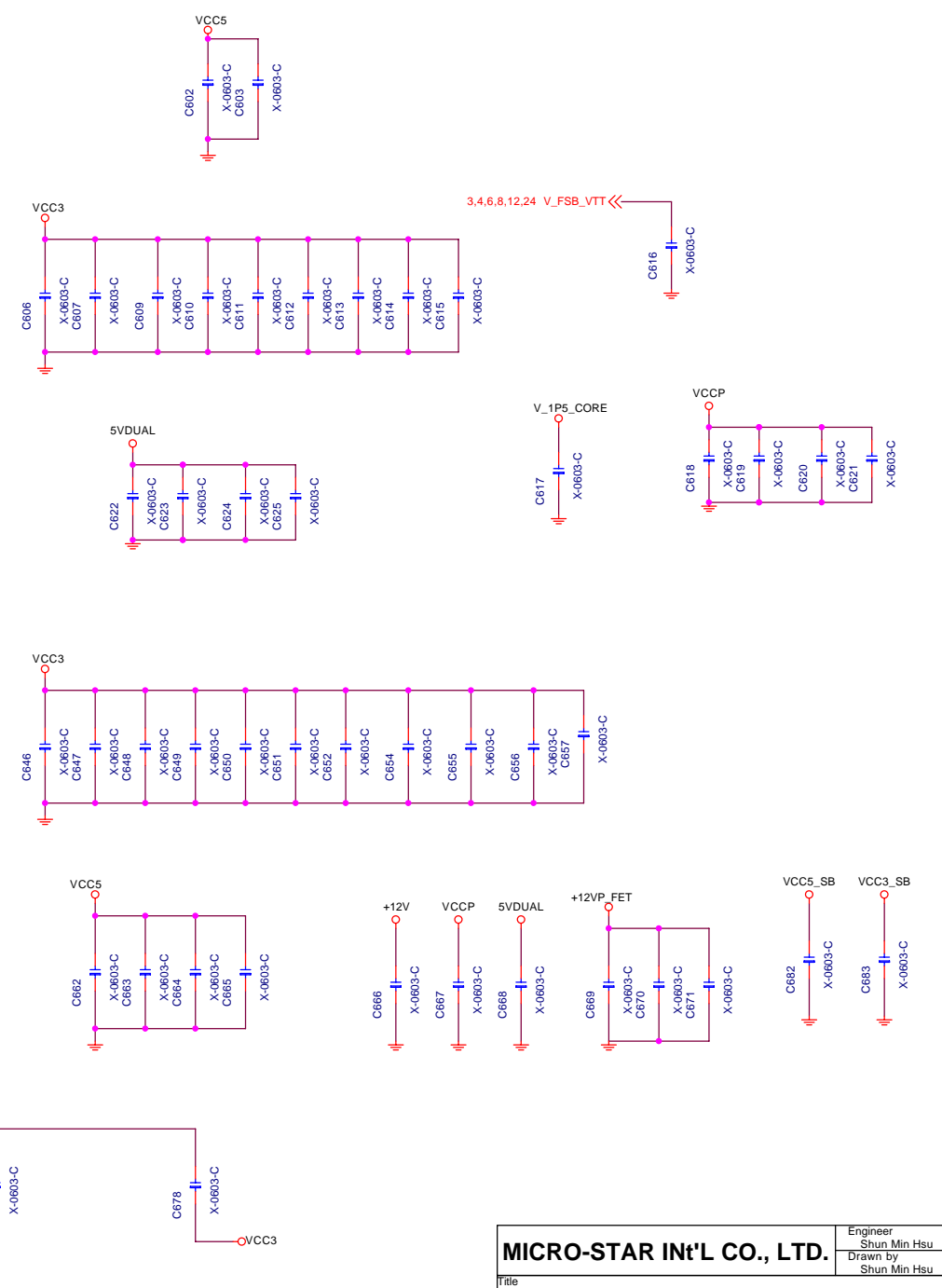
VCC_VID / VID_GOOD
Place MOSFET near CPU

DDR VTT Power

MICRO-STAR INT'L CO., LTD.		Engineer Shun Min Hsu
		Drawn by Shun Min Hsu
Title MS7 ACPI Controller		
Size Custom	Project Name MS-7085	Rev 00
Date: 2004/10/27	Sheet 24	of 27



for EMI



MICRO-STAR INT'L CO., LTD.		Engineer Shun Min Hsu	
Title Misc		Drawn by Shun Min Hsu	
Size A3	Project Name MS-7085	Rev 00	
Date: 2004/10/27	Sheet 25	of 27	

PCI Config.

DEVICE	BUS#	Device#	Function	IDSEL	INT Routing	REQ# /GNT#	CLK GEN PIN OUT
Intel 915GV							
DDR controller	0	0	0	Internal			
Integrated Graphics	0	2	0	Internal	A		
ICH6							
PCI Bridge	0	30	0	Internal			
LPC Bridge	0	31	0	Internal			
IDE	0	31	1	Internal	C		
SATA	0	31	2	Internal			
SM Bus	0	31	3	Internal	B		
AC97 AUDIO	0	30	2	Internal			
USB UHCI 0	0	29	0	Internal	A		
USB UHCI 1	0	29	1	Internal	D		
USB UHCI 2	0	29	2	Internal	C		
USB UHCI 3	0	29	3	Internal	A		
USB 2.0 UHCI	0	29	7	Internal	H		
LAN RTL8101L				AD29	F	REQ# GNT#3	PIN3 (PCI_CLK4)
PCI SLOT				AD16	A	REQ# GNT#1	PIN2 (PCI_CLK3)

ICH6 GPIO

GPIO Pin	Type	Function	Tolerance	Power
GPI 0	I	REQ6#	5V	Core
GPI 1	I	REQ5#	5V	Core
GPI 2	I	PIRQE#	5V	Core
GPI 3	I	PIRQF#	5V	Core
GPI 4	I	PIRQG#	5V	Core
GPI 5	I	PIRQH#	5V	Core
GPI 6	I	Unused	3.3V	Core
GPI 7	I	Unused	3.3V	Core
GPI 8	I	Unused	3.3V	Resume
GPI 9	I	USB_OC4#	3.3V	Resume
GPI 10	I	USB_OC5#	3.3V	Resume
GPI 11	I	SMB_ALERT#	3.3V	Resume
GPI 12	I	Unused	3.3V	Core
GPI 13	I	SIO_PME#	3.3V	Resume
GPI 14	I	USB_OC6#	3.3V	Resume
GPI 15	I	USB_OC7#	3.3V	Resume
GPO 16	O	GNTA#/Unused	3.3V	Core
GPO 17	O	GNTB#/Unused	3.3V	Core
GPO 18	O	Unused	3.3V	Core
GPO 19	O	BIOS_WP#	3.3V	Core
GPO 20	O	Unused	3.3V	Core
GPO 21	O	Unused	3.3V	Core
GPIO 22	N/A	N/A	N/A	N/A
GPO 23	O	Unused	3.3V	Core
GPIO 24	I	SIO SMI#	3.3V	Resume
GPIO 25	O	Strap pin for VCC2_5 regulator	3.3V	Resume
GPI 26	I/O	Unused	3.3V	Core
GPIO 27	I/O	Unused	3.3V	Resume
GPIO 28	I/O	Unused	3.3V	Resume
GPI 29	I	Unused	3.3V	Core
GPI 30	I	Unused	3.3V	Core
GPI 31	I	Unused	3.3V	Core
GPIO 32	I/O	Unused	3.3V	Core
GPIO 33	I/O	Unused	3.3V	Core
GPIO 34	I/O	Unused	3.3V	Core
GPIO39:35	N/A	N/A	N/A	N/A
GPI 40	I	REQ#4	5V	Core
GPI 41	I	LRDQ1#/Unused	3.3V	Core
GPIO47:42	N/A	N/A	N/A	N/A
GPIO 48	O	GNT4#/Unused	3.3V	Core
GPIO 49	OD	CPUPWEGD	V_CPU_IO	Core

Change Note

Ver:0A

2004/07/02

- 1. page13: nopop Q31 Q32 Q33 level shift circuit and change RN77 to 0R
Reserve R508 for VTT_PWRGD# signal
- 2. page20: remove mini-PCI slot
- 3. page23: modify the quantities of bulk caps and MOS
- 4. page24: Remove RAM_HDRV/RAM_HDRV1 circuit.
Modify V_2P5_MCH power sequencing circuit
- 5. page11: SATA2 connect to ICH6 port2
- 6. page12: nopop SM BUS isolation circuit
- 7. page14: connect SMBUS to SIO pin104 and pin105
- 8. page15: Add mute circuit
- 9. page24:Reserve 0603 caps on the GATE of Q30 Q28 Q24 Q23 Q29
- 10. page25: Reserve Caps for EMI

2004/07/12

- 1. page8: Add R517 R516 39.20hm on HSYNC and VSYNC.
- 2. page11: change WAKE# pull-up to VCC3_SB through a 1k ohm resistor.
- 3. page4: Modify CPU VCCA filter circuit.

2004/07/15

- 1. page15: R379 R380 change to nopop.
- 2. page20: Add TPM circuit.
- 3. page10: Reserve R527 for PCI_PME# pullup

2004/07/28

- 1. page26: Add PCI Configuration and GPIO

Ver:0B

2004/08/18

- 1. page14: Swap KBRST# and A20GATE ---- connect to wrong pins on 0A
- 2. page13: Change RN77 to 10Kohm ---- to fix U14 pin51 can not output clock
- 3. page 22: Add R529 on SLP_S3# ---- to avoid SLP_S3#=0.7V when SLP_S3#-->high

2004/08/23

- 1. page21: change CPU FAN connector and add SYSTEM FAN-- For thermal request
- 2. page20: Remove PCI slot -- For thermal request
- 3. page14: Disconnect SIO pin111 and ICH6 pinW6 --- to fix auto power-on issue

2004/08/26

- 1. page14: Change HVCC to VCC3_SB and RN70 connect to VCC3_SB----- For auto power-on problem
- 2. page19: Change J4 to PCMCIA connector ---NEC request
- 3. page13: Add JLPC1 for Debug

2004/08/30

- 1. page22: Reserve C686 C687 C688 C690 For EMI
- 2. page19: Reserve C692 For EMI

2004/08/31

- 1. page14: add RN79 R538 pull up to VCC3_SB because VID[0-4] are input pins

2004/09/03

- 1. page21: add FS4 FS5 on fan control circuit for safety
- 2. page21: change R497 R210 R475 to 10K
change R211 R213 R226 to 5.6K --- adjust FANTACH voltage level to 3V

Ver:0C

- 1. page21: Change FAN connector and add FANTACH swap circuit

MICRO-STAR INT'L CO., LTD.			Engineer Shun Min Hsu	
Title Change Note			Drawn by Shun Min Hsu	
Size	Project Name MS-7085			Rev 0C
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